## REMARKS

Claims 11-25 remain in this application. Claims 11-22 are amended and new claims 23-25 added by this amendment. The title is changed as requested by the Examiner and a Substitute Specification is enclosed. Amended claim 19 no longer contains the laanguage to which the Examiner objected.

Claims 11-18 were rejected as anticipated by Rotenberg and claims 19-22 as obvious over Rottenberg in vie of Patterson. Applicants respectfully traverse these rejections.

One feature of the present invention resides in a decoder circuit selecting an instruction group corresponding to an inputted instruction code based on a history of the inputted instruction code, and uniquely determining an instruction to be executed out of a plurality of executable instructions in accordance with the inputted instruction code. The plurality of executable instructions are sorted into a plurality of instruction groups and each instruction is given with an instruction code different from others within the same instruction group in advance. According to the present invention, it is possible to control the increase in memory capacity required to hold the instruction code, and execute various and advanced processing.

More specifically, conventionally, it is necessary that the executable instructions correspond to instruction codes different from each other. However, in the present invention, with one instruction code corresponding to a plurality of instructions, the instruction to be executed is uniquely selected from a plurality of instructions, based on a history of the inputted instruction codes. Therefore, the present invention can express a plurality of instructions, each from a different group, by the same instruction code, and express many instructions with a shorter instruction code length than the conventional instruction code length.

Contrary to Applicants' claimed invention, Rotenberg discloses what is called a trace cache. As described, Rotenberg combines instructions including a branch instruction in executed order, and stores the combined instructions as one trace with a tag indicating an address of a front instruction (front address of the trace). The purpose of Rotenberg is to shorten latency by using the trace when executing again (trace cache hit). In other words, as one function of the instruction cache, Rotenberg combines executed instructions in sequence and stores them in the cache. The instruction stored in the cache of Rotenberg is usable when executing the same process again.

From the above it becomes clear that the presently claimed invention differs from Rotenberg because Rotenberg does not teach using instructions which are sorted into a plurality

of instruction groups and also fails to teach or suggest that each instruction code is given with an instruction code different from others within the same instruction group, in advance, such as presently claimed. To begin with, Rotenberg does not disclose Applicant's technical concept that it is possible to assign a plurality of instructions to one instruction code, as claimed. Moreover, the description of Rotenberg is simply to combine the instructions stored in a program memory in executed order and store this in a trace cache. Therefore, the arrangement described by Rotenberg can not accomplish the results of the present invention, specifically controlling the increase of memory capacity required to hold the instruction code.

In addition, Rotenberg does not disclose that each instruction group has a certain instruction code to which an instruction belonging to another instruction group can be assigned (As claimed, for example in claims 1 and 19). And Rotenberg does not disclose that a decoder circuit temporarily changes the information corresponding to a history of the inputted instruction code when a certain instruction code is inputted as claimed in claim 14, for example. And Rotenberg does not also disclose an arrangement uniquely determining an instruction to be executed in accordance with a combination of the inputted instruction code and the information corresponding to a history of a plurality of inputted instruction codes (Claim 16, for example.).

In other words each of the independent claims, and thus all dependent claims, contains limitations not taught or suggested by Rotenberg.

Nothing in Patterson et al. makes up for the deficiencies in Rotenberg. The distinguishing features described above are not taught or suggested. Thus, neither alone or in combination do these references teach or suggest what is presently claimed.

In view of the above, all claims remaining in this application are in condition for allowance, prompt notice of which is respectfully solicited.

The Examiner is invited to contact the undersigned at 202-220-4200 to discuss any matter in connection with this application.